ISCAS 2015 TUTORIAL D1

Title: *Event-Based Frame-Free Sensors & Processing: Sensors, Simulators and Hardware Processors.*

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Abstract

Classical artificial vision paradigms produce image sequences with a huge amount of redundant information that must be processed repetitively for extracting useful information for control or decision making. Nevertheless this is not the process that can be seen in biology. A biological retina, for example, continuously signals information changes through spikes to the visual cortex in the brain. This continuous flow of changes in the information allows the human brain to work with only 20W power despite the low speed neuron elements that it uses, and their output spike rate on the order of 10Hz - 100Hz. Since the birth of the concept of neuromorphic engineering in the 90’s, the development of VLSI circuits that mimic the retina, and then the circuits that take advantage of this new representation of the information, have grown and evolved especially in last 10 years. FPGA evolution has accompanied neuromorphic engineering progress and together they are improving the next steps of this philosophy of biological inspiration and mimicking. Today, new large-scale parallel hardware platforms with event-based NoC routing architectures like SpiNNaker, have appeared to support this new processing philosophy. These hardware evolutions are appearing at the same time as interest in the machine learning community in deep neural networks has been exploding and these parallel threads could soon come together. This tutorial will offer attendees (1) the possibility of learning about the principles of the Event-Based Dynamic Vision Sensor Silicon Retina and Event-Based Silicon Cochlea (2) how to take advantage of the output of these continuous flow of events towards a low latency and real time filter implementation for FPGA (like fast object detection and tracking), (3) the basis of functioning and implementation of an event-based convolutional deep networks and some practical applications for Convolutional Neural Networks (ConvNet) on FPGA and (4) an overview of the SpiNNaker platform and robotic applications.

Biographies

**Tobi Delbruck** (IEEE M’99–SM’06–F’13) received the B.Sc. degree in physics and applied mathematics from the University of California, San Diego, and the Ph.D. degree from the California Institute of Technology, in 1986 and 1993, respectively. Currently, he is a Professor of Physics and Electrical Engineering at ETH Zurich in the Institute of Neuroinformatics, University of Zurich and ETH Zurich, Switzerland, where he has been since 1998. His group focuses on neuromorphic sensory processing. He worked on electronic imaging at Arithmos, Synaptics, National Semiconductor, and Foveon. He has co-organized the Telluride Neuromorphic Cognition Engineering summer workshop and the live demonstration sessions at ISCAS and NIPS. He is also co-founder of inilabs and Insightness. Delbruck is past Chair of the IEEE CAS Sensory Systems Technical Committee, current Secretary of the IEEE Swiss CAS/ED Society, and an associate editor of the IEEE TBioCAS. He has been awarded 9 IEEE awards.
Shih-Chii Liu (IEEE M’02–SM’07) studied electrical engineering as an undergraduate and received the Ph.D. degree in the computation and neural systems program from the California Institute of Technology, Pasadena, in 1997. She worked at various companies including Gould American Microsystems, LSI Logic, and Rockwell International Research Labs. She is currently a group leader at the Institute of Neuroinformatics, University of Zurich and ETH Zurich, Switzerland. Her research interests include neuromorphic visual and auditory sensors, cortical processing circuits, and event-based circuits and algorithms. Dr. Liu is past Chair of the IEEE CAS Sensory Systems and Neural Systems and Applications Technical Committees. She is current Chair of the IEEE Swiss CAS/EDSociety and an associate editor of the IEEE Transactions of Biomedical Circuits and Systems and Neural Networks journal.

Alejandro Linares-Barranco (IEEE M’04) received the B.S. degree in computer engineering, the M.S. degree in industrial computer science, and the Ph.D. degree in computer science from the University of Seville (Spain) in 1998, 2002, and 2003, respectively. In 1998 he was Second Lieutenant in the Spanish Air Force as Computer Engineer. From 1998 to 2000, he worked as Technical Staff at the Sevilla Microelectronics Institute (IMSE-CNM-CSIC). From 2000 to 2001, he was a Development Engineer with the R&D Department, at SAINCO-Telvent (ABENGOA group). Since 2001 to 2006, he was an Assistant Professor at the Computer Architecture and Technology Department of the University of Seville. In 2006 he was promoted to Associate Professor. His Lab (Robotics and Computers Technology) developed a set of AER-tools for debugging and connecting AER systems under the EU project CAVIAR. His research interests include VLSI and FPGA digital design, neuro-inspired chip-to-chip and chip-to-computer interfaces, spike and event-based processing, motor control and vision for FPGAs, wireless sensor networks and embedded applications based on microcontrollers, bus emulation, and computer architectures. In the last years he and RTC lab have developed several event-based processing blocks for event-based vision and event-based motor control in the context of the Spanish research projects VULCANO (TEC2009-10639-C04-02) and BIOSENSE (TEC2012-37868-C04-02) where he served and PI for the RTC partner. He is member of the Technical Committee on Neural Systems and Applications (NSATC) and Sensory System TC of the IEEE Circuits and Systems Society. He is past chair of NSATC.

In 2014 he was visiting professor at ETH/UZH and a collaborator of the Institute of Neuroinformatics for the EU VISUALISE project, where retina ganglion cells models are implemented on FPGA with event-based processing for neuromorphic vision sensors.

Bernabé Linares-Barranco (IEEE F’10) received the B.S. degree in electronic physics, the M.S. degree in microelectronics, and a first Ph.D. degree in high-frequency OTA-C oscillator design from the University of Sevilla, Sevilla, Spain, in 1986, 1987, and 1990, respectively, and a second Ph.D. degree in analog neural network design from Texas A&M, College Station, in 1991. Since September 1991, he has been a Tenured Scientist at the Sevilla Microelectronics Institute (IMSE), which is one of the institutes of the National Microelectronics Center (CNM) of the Spanish Research Council (CSIC) of Spain. On January 2004 he was promoted to Full Professor of Research. He is participating in a number of EU funded projects, including the FET-Flagship “The Human Brain Project”. He has been involved with circuit design for telecommunication circuits, VLSI emulators of biological neurons, VLSI neural-based pattern recognition systems, hearing aids, precision circuit design for instrumentation equipment, bio-inspired VLSI vision processing systems, transistor parameter mismatch characterization, address-event-representation VLSI, RF circuit design, real-time vision processing chips, and extending AER to the nanoscale. Dr. Linares-Barranco has received several IEEE Best Paper awards. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS and of the IEEE TRANSACTIONS ON NEURAL NETWORKS. He is an Associate Editor of Frontiers in Neuromorphic Engineering. From March 2011 until October 2013 he was Chair of the IEEE CAS Society Spain Chapter.
Steve B. Furber (IEEE F’05) was born in Manchester, U.K., in 1953. He received the B.A. degree in mathematics and the Ph.D. degree in aerodynamics from the University of Cambridge, U.K., in 1974 and 1980, respectively, and honorary doctorates from Edinburgh University, Edinburgh, U.K., in 2010 and Anglia Ruskin University, Cambridge, U.K., in 2012. From 1978 to 1981, he was Rolls Royce Research Fellow in Aerodynamics at Emmanuel College, Cambridge, U.K., and from 1981 to 1990, he was at Acorn Computers Ltd., Cambridge, U.K., where he was a principal architect of the BBC Microcomputer, which introduced computing into most U.K. schools, and the ARM 32-bit RISC microprocessor, over 50 billion of which have been shipped by ARM Ltd.’s partners. In 1990, he moved to the ICL Chair in Computer Engineering at the University of Manchester, Manchester, U.K., where his research interests include asynchronous digital design, low-power systems on chip, and neural systems engineering. Prof. Furber is a Fellow of the Royal Society, the Royal Academy of Engineering, the British Computer Society, the Institution of Engineering and Technology and the Computer History Museum (Mountain View, CA). He was a Millennium Technology Prize Laureate (2010) and holds an IEEE Computer Society Computer Pioneer Award (2013).

Jörg Conradt (M’09) is Junior Professor at the Technische Universität München in the Faculty of Electrical Engineering and Information Technology, Institute of Automation and Control Engineering. The laboratory is affiliated with TUM’s Competence Center on NeuroEngineering and the Munich Bernstein Center for Computational Neuroscience. He holds an M.S. degree in Computer Science/Robotics from the University of Southern California, a Diploma in Computer Engineering from TU Berlin and a Ph.D. in Physics/Neuroscience from ETH Zürich. His research group on Neuroscientific System Theory (http://www.nst.et.tum.de) investigates key principles by which information processing in brains works, and applies those to real-world interacting technical systems.