ISCAS 2015 TUTORIAL M1

Title: Design Methodology and Circuit Techniques for Any-Load Stable LDO Regulators with Instant Load Control

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Abstract

Application of the structural methodology to the LDO design creates a new class of circuits: any load stable, with instant transient response, large power supply rejection ratio and low noise. Presented are examples of the imbedded in SoC LDOs for the SRAM unit, (5 ns reaction time on the load steps), radio transmitter (shaping the required noise vs. frequency characteristic) and LDO for memory retention in the shutdown state (300 nA quiescent current). These LDOs can operate with or without off-chip load capacitors; they are robust to the process and temperature variations and portable to any CMOS process. The circuit techniques demonstrated during this course is proven in design of industrial circuits including LDO regulators.


Biographies

Vadim Ivanov received the M.S.E.E. degree and the Ph.D. degree in 1987, both in the USSR. He designed electronic systems and ASICs for naval navigation equipment from 1980 till 1991, and mixed signal ASICS for sensors, GPS/GLONASS receivers and motor control circuits from 1991 till 1995 in St. Petersburg, Russia. He joined Burr Brown (presently Texas Instruments in Tucson) in 1996 as a senior member of technical staff where he designed operational, instrumentation and power amplifiers, and voltage references as well as switching and linear voltage regulators. He has more than 60 US patents on applications of analog circuit techniques. He also authored about 30 technical papers and three books: Power Integrated Amplifiers (Leningrad, Rumb, 1987), Analog
System Design Using ASICS (Leningrad, Rumb, 1988), both in Russian, and Operational Amplifier Speed and Accuracy Improvement (Kluwer, 2004).